averaging means for averaging an output signal of said addition means along a time axis;

decision means for outputting a decided signal of received data by performing received phase error compensation on the output signal of said integral means;

inverse modulation means for inversely modulation an output signal of said averaging means by said decided signal; and

clock generating means for outputting a clock signal whose phase is controlled by a phase error signal outputted from said inverse modulation means,

wherein said replica generating means is driven by said clock signal generated by said clock generating means.

8. The CDMA communication system as claimed in claim **7**, further comprising:

initial acquisition means including tapped storing means for storing said received signal of at least one spreading code interval long, tap coefficient means for storing said despreading code, fourth multiplication means for multiplying individual chips stored in said tapped storing means by stored patterns of said despreading code stored in said tap coefficient means, and second addition means for summing outputs of said fourth multiplication means; and

switching means for supplying said received signal to said initial acquisition means when a phase difference between said received signal and said despreading code is greater than a predetermined value, and for supplying said received signal to said tracking means when said phase difference is smaller than said predetermined value.

9. A receiver for a CDMA communication system including a plurality of the receivers, each of the receivers being provided with a tracking means for maintaining synchronization between a received signal and a despreading code by suing a correlation between the received signal and the despreading code, the received signal being CDMA spread and received by the receiver, and the despreading code being used for despreading the received signal, said tracking means in the receiver comprising:

replica generating means for generating a phase advanced replica of a CDMA spreading code with an advance phase with respect to said received signal, a phase retarded replica of the CDMA spreading code with a retarded phase with respect to said received signal, and a phase synchronized replica of the CDMA spreading code with synchronized phase with respect to said received signal;

first multiplication means for multiplying said received signal by said phase advanced replica;

second multiplication means for multiplying said received signal by said phase retarded replica;

a first filter for extracting from an output signal of said first multiplication means a correlation detection signal indicating a correlation between said phase advanced replica and said received signal;

a second filter for extracting from an output signal of said second multiplication means a correlation detection signal indicating a correlation between said phase retarded replica and said received signal;

third multiplication means for multiplying said received signal by said replica in synchronism with said received signal;

integral means for integrating an output signal of said third multiplication means over M chip intervals;

automatic frequency control means for detecting said carrier frequency error from an output signal of said integral means, and for compensating for said carrier frequency error;

carrier frequency error compensation means for compensating for a carrier frequency error associated with said first and second correlation detection signals;

addition means for summing in opposite phase said output of said first filter and said output of said second filter, which have been compensated by said carrier frequency error compensation means;

averaging means for averaging an output signal of said addition means along a time axis;

decision means for outputting a decided signal of received data by performing received phase error compensation on the output signal of said integral means;

inverse modulation means for inversely modulation an output signal of said averaging means by said decided signal; and

clock generating means for outputting a clock signal whose phase is controlled by a phase error signal outputted from said inverse modulation means,

wherein said replica generating means is driven by said clock signal generated by said clock generating means.

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